

Curriculum Vitae

Name & Qualification	Dr. KHALIL-UR-REHMAN DAYO Assistant Professor Father's Name: Faiz Mohammad Dayo Contact No. +92 332 2367304 CNIC: 41204-3251597-9  Ph.D (VLSI/ FPGA) [Mehran University of Engg. & Tec:/ Nanyang Technological University SINGAPORE] Ph.D Thesis Title "Logic Decomposition with Technology Mapping for Area and Delay Minimization in FPGA Design" 2007 Jointly supervised by NTU Singapore & Mehran University of Engg. & Tech: Supervisors.	E-Mail: Khalil.dayo@faculty.muett.edu.pk  M.E (Telecom & Control Engg) 2001 Master Thesis "Software Development And Statistical Analysis Of Relative Performances For B.I.S.Es, With I.B.A (Test score) Karachi" 2001.  Postgraduate COC Diploma CTC Islamabad 1999. PG Project: Computer Networks  B.E (Electrical Engineering) Bachelors Thesis "Role of Fiber optics in Modern Telecommunication System" 1993.
Major Trainings / Workshops Attended with (Test/quizzes/ Final Exam:)	➤ Integrated Circuits Design (04 Feb. 2013 to 08 Feb. 2013) @ National Institute of Electronics Islamabad (NIE) [Software used Pyxis Schematic/ Pyxis Layout, ModelSim, Leonardo Spectrum synthesizer, Eldo Simulator] ➤ IC Design Flow with IC Studio (31 August 2009 to 03 Sep: 2009) @ Mentor Graphics SINGAPORE. ➤ Custom Training (DX Designer & Expedition) (04 Sep: 2009 to 08 Sep: 2009) @ Mentor Graphics SINGAPORE. ➤ FPGA Advantage (09 Sep: 2009 to 11 Sep: 2009) @ Mentor Graphics SINGAPORE. ➤ VLSI Design Techniques (Two weeks Training workshop, April 2003 @ Computer Training Centre Islamabad) ➤ Oracle: SQL & PL/ SQL (Two weeks course organized by National Institute of Public Administration NIPA, Karachi) April 2001. ➤ SIX MONTHS Postgraduate (June 1999 to Nov: 1999) @ Computer Training Centre Islamabad. (Courses/Software& O.S : Visual Basic, Unix, MatLab, AutoCAD, MIS, Computer Architecture, Computer Networking)	
Teacher's Professional Course	✓ Professional Competency Enhancement Program For Teachers (PCEPT)	04 Weeks Course Certificate awarded by; National Academy of Higher Education, HEC Islamabad (15 Sep:2010 to 14 Oct: 2010)
Teaching Experience (Bachelor's Level)	32 Years Teaching Experience in Various Departments Education deptt. Govt. of Sindh, Electrical Engineering, Electronic Engg., Computer Engg., Telecommunication Engg., Bio-Medical Engg., Mechatronic Engg. Mehran University of Engg. & Tech.	SUBJECTS: (Theory & Practical) FPGA Based System Design, Integrated Circuits, Microprocessor & Interfacing Techniques, Microcontroller & Embedded systems Sequential Circuits Design, Communication system , Digital Logic & Design.....
Teaching Experience Postgraduate Level)	20 years Master/ PhD Teaching Experience in various Postgraduate Programs, ○ Telecommunication & Control Engg: ○ Electronic System Engineering (ESE) ○ Telemedicine ○ Mechatronics ○ Embedded System Design	Advanced Microprocessor based System Design, Semiconductor Material & Technology, I.C Design & Manufacturing Techniques, Digital Integrated Circuits for Communication Design, Computer Networks, Advanced FPGA based System Design (Practical Labs on FPGA Advantage by: Mentor Graphics), Advanced I.C Design, , Data Acquisition & Control, Advanced Embedded systems.....

Publications	➤ Tanesh Kumar, Khalil-ur-Rehman Dayo, Pardeep Kumar, B.S Chowdhry and Bishwajeet Pandey ; “Thermal Aware Energy Efficient ALU Design on Different FPGA” NED UNIVERSITY JOURNAL OF RESEARCH, Special issue on MCCT'14; 2015. pp. 93-104. ➤ Tanesh Kumar, Pardeep Kumar, Khalil-ur-Rehman Dayo, B.S Chowdhry and Bishwajeet Pandey ; “LVTTL IO STANDARDS AND CAPACITANCE SCALING BASED ENERGY EFFICIENT ALU DESIGN ON FPGA” NED UNIVERSITY JOURNAL OF RESEARCH, Special issue on MCCT'14, 2015 pp. 39-47. ➤ Tanesh Kumar, Bishwajeet Pandey, Kr Dayo, B.S Chowdhry and Pardeep Kumar, “LVTTL Based High Performance Energy Efficient 64-bit ALU Design on FPGA” International Conference on Modern Communication & Computing Technologies - MCCT'14 QUEST Pakistan: Feb. 2014. ISSN number 2311-5297 ➤ Tanesh Kumar, Bishwajeet Pandey, Kr Dayo, B.S Chowdhry and Pardeep Kumar, “Thermal Aware Energy Efficient ALU Design on Ultra Scale FPGA” International Conference on Modern Communication & Computing Technologies - MCCT'14 QUEST Pakistan: Feb. 2014. ISSN number 2311-5297 ➤ KHALIL-UR-RAHMAN DAYO, AND TAYAB DIN MEMON “Ternary and Multi-Bit FIR Filter Area-Performance Tradeoffs in FPGA” , Mehran University Research Journal of Engineering & Technology, Volume 32, No. 1, January, 2013 [ISSN 0254-7821] ➤ TAYAB DIN MEMON, BHAWANI SHANKAR CHOWDHRY, AND KHALIL-UR-RAHMAN DAYO “Sigma Delta Modulation Based Ternary FIR Filter Mapping on FPGA” Mehran University Research Journal of Engineering & Technology, Volume 30, No. 3, July, 2011 ➤ Bhawani Shankar Chowdhry, NeilWhite, Jai Kumar, Khalil Dayo, “Vissualization& Analysis of Wireless Sensors Network Data for Smart Civil Structure on special correlation Technique” , American Institute of Physics Journal 2009. ➤ Khalil Dayo, Qadeer Rajput , Bhawani Chowdhry “Impact of Cluster Size on Efficient LUT-FPGA Architecture for Best Area and Delay Trade-off” IMTIC 2008, CCIS 20, pp. 243–252, 2008. Springer-Verlag Berlin Heidelberg 2008. ➤ Dayo, K.R., Rajput, A.Q.K., and Chowdhry ,B.S, “Analysis and Comparison of Synthesizing Algorithms for Area and Delay Minimization in FPGA Architecture”, Mehran University Research Journal of Engineering & Technology, Volume 25, No. 4, , Jamshoro, Pakistan, pp 351- 362 October, 2006 ➤ Dayo, K.R., Rajput, A.Q.K., Chowdhry, B.S., and Siyal, M.Y, “Investigating the Synthesis Algorithms for Area and Delay Minimization in FPGA Design” IEEE, pp 29-35, Vol No. 46-47, 2005.
Additional Professional Assignments	✓ Ex-Chairman QEC Electronic Engineering Mehran University of Engg. & Tech. ✓ Ex-Member National Curriculum Revision Committee HEC Islamabad (NCRC) (Electronic Technology) (2009-2012) ✓ Member Pakistan Engineering Council Registration No. ELECT/10761 ✓ Periodically Chairman, Electronics Engineering Department; (During HOD`s Foreign visits) ✓ Developing Database Projects officially assigned by university authorities. ✓ Microcontroller/Microprocessor Programming using Assembly Language. ✓ Verilog/ VHDL based projects.